of the floating gate;[, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and]

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the [until the second thickness is substantially equal to the first thickness, whereby polishing the insulator produces a] floating gate and the insulator layer; and

depositing a dielectric layer directly on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

2. (Amended) The method of claim 1, wherein the insulator layer comprises [is a high quality] a furnace grown oxide.

3. (Amended) The method of claim 1, wherein the [first] thickness of the floating gate is [no more than approximately] between approximately 500 Å and 2000 Å, and the [second] thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

4. (Amended) The method of claim 1, wherein polishing the insulator layer includes chemical mechanical polishing.

5. (Amended) The method of claim 1, further comprising:

[depositing a dielectric layer on the floating gate and insulator layer;]

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

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7. (Amended) A method of making a flash memory cell having a substrate and a tunnel oxide formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide to[, the floating gate layer having] a first thickness;

etching the floating gate layer, to provide a floating gate;

forming an oxide on exposed surfaces of the floating gate;

depositing an insulator layer on the substrate[, the insulator covering the] and the floating gate[, a portion of the insulator not covering the floating gate having a second] such that the insulator layer has a thickness that is greater than the first thickness; [and]

polishing the insulator layer to provide a planar surface that exposes a top surface of the [until the second thickness is substantially equal to the first thickness, whereby polishing the insulator produces a] floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

8. (Amended) The method of claim 7, wherein the insulator [is a high quality] comprises a furnace grown oxide.

9. (Amended) The method of claim 7, wherein the first thickness is [no more than] between approximately 500Å and 2000 Å, and the [second] thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

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10. (Amended) The method of claim 7, wherein polishing the insulator layer includes chemical mechanical polishing.

11. (Amended) The method of claim 7, further comprising:

[depositing a dielectric layer on the floating gate and insulator layer;]

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

A2 cont

REMARKS

Claims 1-15 were pending prior to the above amendments. Claim 13 is canceled. Claims 1-5 and 7-11 are amended to more particularly point out and distinctly claim Applicants' invention.

The Examiner rejected Claims 1-15 under 35 U.S.C. § 112, second paragraph, as being indefinite. As amended, Applicants respectfully submit that the Examiner's objections are overcome.

The Examiner rejected Claims 1-2, 4-8 and 10-12 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,962,889 ("Yamauchi"). The Examiner states:

> Yamauchi et al. discloses a method for forming a semiconductor device, which comprises providing a substrate 1; forming tunnel oxide 2 on the substrate; depositing a floating gate layer on the tunnel oxide, the floating gate layer having a first thickness; etching the floating gate layer to form floating gate 3; depositing an insulator 7 on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness; and polishing the insulator until the second thickness is substantially equal to the first thickness,

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